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# Indium Tin Oxide Fabricated at Low Energy Consumption Conditions for Silicon Solar Cell Technology

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**Abstract:** In this work, thin indium tin oxide (ITO) films deposited under low energy consumption conditions were investigated to be used with different roles in silicon-based device technology. All the ITO layers were fabricated by direct-current magnetron (DC) sputtering. The first role consisted of an effective n-type doped layer to be used in a n-p heterojunction. In this case, the thin films were deposited at room temperature and an applied DC power of 25W on p-type crystalline silicon substrates, varying their thickness from 45 to 140 nm. The second role evaluated was as an antireflective electrode. ITO was incorporated as front contact on silicon heterojunction solar devices. In this case, the substrate temperature was set to 190ºC and room temperature, respectively, while the applied DC power was varied from 25 to 75 W. We show the impact of the nature of the ITO, its thickness, and the sputtering conditions on the main device parameters, such as short-circuit current density and open-circuit voltage. The results indicate that these ITO thin films fabricated at low energy consumption conditions present adequate performance to be used as conventional emitters and front contacts in silicon technology without using heat treatment processes, respectively.

**Keywords:** ITO; magnetron sputtering; low temperature; silicon-based photovoltaic devices.



## 1. Introduction

Transparent conductive oxide (TCO) materials such as indium tin oxide (ITO), aluminum-doped zinc oxide (AZO), cadmium oxide (CdO), or tin oxide ($SnO_2$) are extensively used in a wide range of optoelectronic devices such as flat panel displays, photovoltaic cells, light-emitting diodes, semiconductor lasers or low emissivity windows [1-3]. They must simultaneously exhibit high performance in visible-range transparency and conductivity. Thanks to these properties, TCOs are a necessary and essential component in photovoltaic (PV) devices. It is known that the coexistence of both properties in a TCO depends on its nature, its number and atomic arrangements of metal cations, its morphology, and the presence of intrinsic or introduced defects in it. The TCOs present several roles on the devices. Among others, they can act as (i) transparent electrodes, (ii) structural templates, and/or (iii) diffusion barriers [4].

In addition, their properties can exert influence on the PV cell parameters, such as the open-circuit device voltage Voc or the short-circuit current Jsc, and hence, they contribute directly to the device performance. TCOs for terrestrial PV applications must use low-cost materials, and some may require device-technology-specific properties. Among the TCOs, the most widely used material today remains ITO [5]. 100 nm-thick of this TCO presents sheet resistances as low as 10 Ω/sqr and transmittance in the visible wavelength >90% [6]. Magnetron sputtering is a large-area deposition technique that gives adequate quality ITO layers and is more flexible for controlling the film properties. This technique permits the deposition at low temperatures, and the layers present excellent adherence to the substrate. Despite the achievements with ITO, the high cost of indium due to its scarcity is motivating the investigation of other substitute materials [7]. However, ITO continues to be the predominant one because of its ease of processing. So far, no TCO has succeeded in improving its optoelectronic properties. The problem with the scarcity of indium is currently being solved by recycling it. Due to the new environmental policy of circular economy [8,9], many companies are offering to recycle and reclaim programs for this material [10-12]. Hence, the consumption of indium is being reduced. Despite all these efforts, the indium shortage may occur in the next few years if environmental policies do not apply. On the other hand, in most of the manufactured products that incorporate ITO in their production chain, post-deposition treatments are required to achieve high-quality ITO thin films with adequate electronic properties retaining high transparency [13]. In the case of PV sector, the next generation of devices demands cost-reduction products and reduction of both energy and material losses. Low-temperature fabrication processes are preferred. They must be compatible with thinner and/or lower-quality wafers [14].

In this work, the role of ITO as (i) an effective n-doped layer in a heterojunction acting as a selective carrier layer, (ii) a transparent electrode, and/or (iii) an antireflection coating (ARC) in silicon-based PV devices is evaluated and demonstrated. The ITO thin films are fabricated at low energy consumption conditions without any post-heat treatment to reduce the energy manufacturing consumption and diminish the production cost for that PV technology.

## 2. Materials and Methods

ITO thin films were fabricated using a commercial UNIVEX 450B system from Leybold. This system is equipped with magnetron sources, two of them are operated by Radio Frequency (RF), and the other two are operated by direct current (DC). The four guns are placed in a confocal geometric configuration around 0,15m from the substrate center. This special geometry assesses the homogeneity of the fabricated films. The 4-inch diameter $SnO_2$:$In_2O_3$ ceramic target was placed on a direct current (DC) source. The target was provided by Neyco, and it had a nominal composition of 10/90 wt % with a purity of 99.99%.

Two different substrates were used depending on the role of the ITO layer: resistive corning glass to obtain the optical performance of the films in the visible range and three different silicon wafers: polished resistive float zone (FZ) <100> silicon wafer (resistivity>$10^4$ Ω-cm) to determine the antireflection role and its electrical conductivity, double-polished FZ p-type silicon wafers (resistivity ~ 1000-5000 Ω-cm) to be used as absorber in the N-P heterojunction, and double side polished Czochralski (CZ) 280 µm N-type wafer to be used as an absorber in the SHJ solar cells.

The sputtering process was performed in an oxygen-free environment with a base pressure of 1x$10^{-5}$ Pa. The inert gas used was Argon, which has a purity of 9N5. The gas flux

was controlled by a MKS mass flow controller, while the gas flow rate and the working pressure were set to 5 sccm and 0.17 Pa, respectively. During the deposition, the substrate was rotated at 20 rpm. The DC power (DCP) values ranged from 25 to 75W, and the substrate temperature varied from room temperature (RT) to 190ºC.

The structural composition of the thin films was determined by X-ray diffraction (XRD). The patterns were obtained using a PANalytical X'Pert Pro diffraction system configured with a vertical Theta. wide-angle goniometer, that operates in grazing incidence (GI) configuration, using. a Goebel-type parallel beam mirror on the incident beam side and a linear X'Celerator detector in receiving slit mode attached to a parallel plate collimator on the diffracted beam side. The radiation was $CuK_\alpha$ (45 kV - 40 mA) at a fixed incident angle of $\omega$= 2.5º in parallel beam geometry in an angular range of $20° < 2\theta < 80°$. The Inorganic Crystal Structure Database (ICSD) was used for the phase identification. The elemental composition of ITO layers was determined with wavelength dispersive X-ray fluorescence analysis (WDXRF) measured using a PANalytical AXIOS automated XRF spectrometer. The samples were analyzed using a semiquantitative (OMNIAN) method developed by PANalytical. Film morphology was analyzed with a Digital Instruments Nanoscope IIIa Atomic Force Microscope in tapping mode with Bruker NCHV probes, and the scans were processed using Nanotec software WSxM [15]. Hall mobility and carrier concentration were carried out under a 1.2 T magnetic field with the Van der Pauw method at RT. Optical transmittance (T) at the wavelength range from 300 to 2500 nm was measured at RT and normal incidence using a UV/Visible/NIR Perkin-Elmer Lambda 1050 spectrophotometer. The anti-reflective (AR) capability of the thin films was determined from the hemispherical reflectance spectrum Rhem measured with the UV/VIS/NIR Perkin-Elmer Lambda 1050 spectrophotometer equipped with the 6 mm integrated sphere accessory.

In this work, two types of devices were fabricated. The first one is ITO-based N-P heterojunction protocells onto the polished FZ p-type silicon substrates, where ITO can play the main role of the n-type emitter. The silicon wafer was dipped in HF to remove the native oxide before loading it into the sputtering chamber to deposit the ITO layer. A metallic grid of Ti (55 nm)/Ag (1µm) was evaporated as the front contact and 900 nm-thick aluminum as the rear contact. To achieve the ohmic behavior, this last one was previously annealed at 350 ºC for 2 hours in an Argon environment.

The second device consisted of a silicon heterojunction solar cell (SHJ) where ITO plays the double role of an ARC and front electrode. The wafer was also dipped in HF before loading into an Elettrorava s.p.a. plasma-enhanced chemical vapor deposition system operating at 13.56 MHz. Both sides of the wafer were passivated by a very thin layer of intrinsic amorphous silicon (a-Si:H) deposited from a pure $SiH_4$ plasma. After that, back- and front-side emitters were deposited from a $SiH_4$ and $PH_3$ or $B(CH_3)_3 + H_2$ plasma to ensure good majority and minority carrier collection. The back of the wafer was then fully covered with a Ti+Ag metal electrode, while on the front side, 80 nm of ITO were deposited. Finally, both devices were completed with the evaporation of a Ti+Ag metal grid on top of the ITO layer.

The devices' current-voltage (JV) characteristics were measured under illumination, AM1.5G conditions, and 100 mW/cm$^2$, using a class A solar simulator (Steuernagel SC575). Suns-Voc measurements were carried out with the Sinton Instrument WCT-120 and the appropriate accessory stage to evaluate the effect of the ITO layer on the passivation layer.

## 3. Results and Discussion

In this section, we show the main results obtained from the different roles of ITO thin films.

### *3.1. ITO as n-layer in a N-P silicon heterojunction protocell.*

Figure 1 pictures the GI-XRD scans of as-deposited ITO thin films at the soft conditions of 25 W of DCP and RT fabricated onto the corning glass. The nominal film thickness ranged from 45 to 140 nm. A transition from amorphous to polycrystalline (pc) nature happened when the film thickness was slightly higher than 80 nm. At this thickness, a very weak peak around 30º began to appear in the scan, hidden in the broad hump corresponding to the amorphous glass.

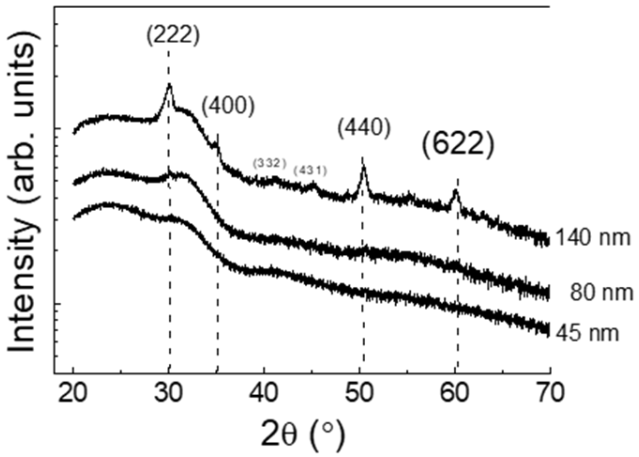


**Figure 1.** GI-XRD scans of ITO thin films, varying the thickness, deposited at soft conditions.

With regards to the 140 nm-thick film, the XRD scan showed four main peaks corresponding to the (222), (400), (440), and (622) planes. Among them, the (222) plane, corresponding to the cubic bixbyite $In_2O_3$, presented the maximum intensity, indicating this was the preferred orientation. No characteristic peaks of tin (Sn), SnO, or $SnO_2$ appeared in the scans, meaning that the hosting of Sn in the substitutional position of the $In_2O_3$ cubic lattice successfully happened [16]. However, the chemical composition (in percentage) was estimated from WD-XRF measurements, showing traces of Sn compounds. Regardless of the layer thickness, the percentage of $In_2O_3$ was 87.8 and of $SnO_2$, 12.2, slightly higher than the nominal composition of the ceramic target.

Table 1 shows the electrical parameters (carrier density n, mobility μ, and sheet resistance Rsheet) obtained from Hall measurements as a function of the thickness of the ITO deposited onto resistive FZ silicon wafers.

**Table 1.** Electrical parameters of ITO thin films fabricated at 25W and RT, as a function of the thickness.

| Thick (nm) | Hall electrical parameters | | |
|---|---|---|---|
| | n ($10^{20}$cm$^{-3}$) | μ (cm$^2$/V·s) | $R_{sheet}$ (Ω/sqr) |
| 45 | 6.20 | 20.2 | 260 ± 6 |
| 80 | 7.20 | 16.0 | 85 ± 5 |
| 140 | 4.20 | 25.5 | 55 ± 5 |

As the thickness increased and the crystalline transition occurred (at around 80 nm-thick), the n concentration drastically decreased while the mobility μ sharply increased, denoting a reversed trend between them [17]. Regarding the carrier concentration, a resulting

sharp drop was observed at the transition point. This could be explained because, in the case of amorphous thin films, the Sn doping did not contribute to generating carriers [18]. However, in the 140 nm-thick pc film, the Sn atoms diffuse from interstitial to cation sites, producing a realignment of In-O bonds would be happening to generate a locally ordered structure. Hence, the mechanism of providing carriers was different, and no relationship could be established at the transition point. The higher mobility measured in the pc film might be related to the crystalline improvement and the effect of the lattice modifications resulting from doping content reached when thickness increased. Additionally, the sheet resistances decreased when the layer thickness increased, agreeing with theoretical predictions [19].

Figure 2 shows the transmittance spectra of the samples in the study. The spectrum of the corning glass substrate is also included.

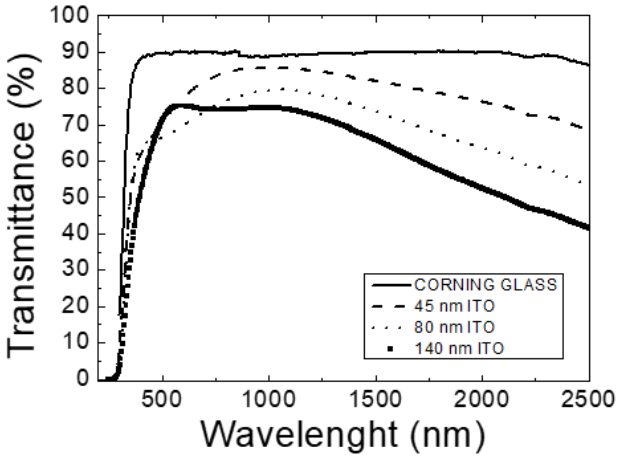


**Figure 2**. Transmittance spectra of ITO thin films varying the thickness deposited at soft conditions.

The normalized average transmittance values in the 400-1000 nm wavelength region were higher than 80 % in all cases (specifically, 89% for 45 nm-thick, 82% for 80 nm-thick, and 81% for 140 nm-thick). In addition, the decrease in transmittance in the near-infrared region (NIR) region was observed while thickness increased [20].

Figure 3 depicts the J-V characteristics measured under the illumination of the protocells fabricated incorporating the ITO films of different thicknesses.

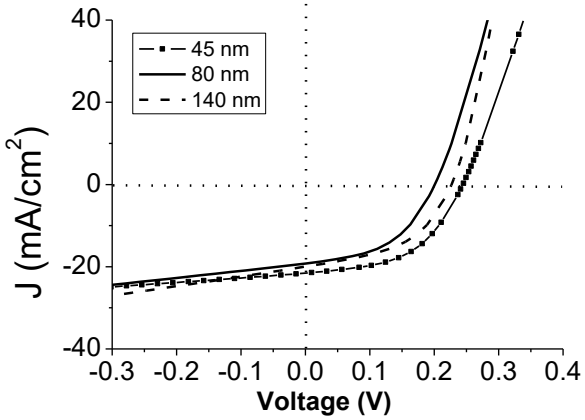


**Figure 3**. J-V characteristics under illumination of ITO/p-Si devices as a function of ITO thickness. ITO layers were fabricated at 25 W and RT.

It should be highlighted that no passivation layer was used in the device because the main goal consisted of evaluating the effect of the ITO film thickness on the device's

performance, thanks to its capability as a carrier transport layer. Due to the lack of passivation layer, the Voc values obtained were much lower than the common ones for silicon-based technology. A stronger influence on Voc was observed, varying the ITO thickness in the range of 45 to 140 nm, as showed the data in Table 2.

**Table 2.** Open-circuit voltage Voc and short-circuit current Jsc extracted from J-V characteristics under the illumination of the protocells fabricated as a function of ITO thickness.

| ITO thickness (nm) | Voc (V) | Jsc (mA/cm$^2$) |
|---|---|---|
| 45 | 0.25 | 21.4 |
| 80 | 0.20 | 19.2 |
| 140 | 0.23 | 19.8 |

The highest Voc value was achieved by using a 45 nm-thick ITO layer. This can be related to the film mobility and should indicate the effective transport of photogenerated electrons. The slight difference observed in the Voc of the devices fabricated with 45 nm-thick (amorphous layer) and 140 nm-thick films (pc layer) was attributed to (i) the nature of the thin film, (ii) the effect of grain boundary scattering in the pc-film, and (iii) the band alignment modified with the carrier concentration [21]. Although the amorphous film presented lower mobility than the pc one (20.2 cm$^2$/Vs vs 25.5 cm$^2$/Vs), this effect could be compensated by the non-existed boundary grains, hence, scattering at them. Therefore, the electrons could flow easily from the active layer. Regarding the Jsc, no systematic trend was shown, with ITO thickness being slightly higher in the case of using 45 nm-thick ITO layer.

*3.2. ITO as ARC and front electrode in a silicon heterojunction solar cell.*

Sputtered ITO thin film is commonly used as front contact for the current collection in SHJ technology. However, many studies show that the sputtering fabrication process affects the properties of the a-Si:H passivation layer and hence, device performance [22,23]. In this work, two different DCP values of 25 and 75W and two substrate temperatures of RT and 190ºC were used to fabricate the 80 nm-thick ITO layer. The main objective is to evaluate the effect of the sputtering conditions on device performance.

The GI-XRD scans of the as-deposited 80 nm-thick ITO thin films (not shown) [24] showed an amorphous to crystalline transition when DCP value increased from 25W to 75W. At RT, the spectrum for the film deposited at 25 W presented a broad hump around 31º, revealing its amorphous nature. This means that due to these soft growth conditions, the change in kinetic energy of the particles reaching the growth front was not enough to favor the (400) orientation [24]. Otherwise, the scans of samples deposited at 75 W showed a pc structure with (222), (400), (440), and (622) diffraction peaks. The (222) reflection corresponding to the cubic bixbyite $In_2O_3$ presented the maximum intensity, indicating the preferred orientation. Upon increasing the substrate temperature to 190 ◦C, the peaks observed in the films deposited at RT were almost non-existent with very low intensity. Instead, a new intense diffraction peak corresponding to the (611) crystalline plane was detected. This (611) orientation predominated because of the higher growth rate of such crystals compared with other directions as substrate temperature increased [25].

Figure 4 depicts the 2D AFM micrographs of the 80 nm-thick ITO films in the study.

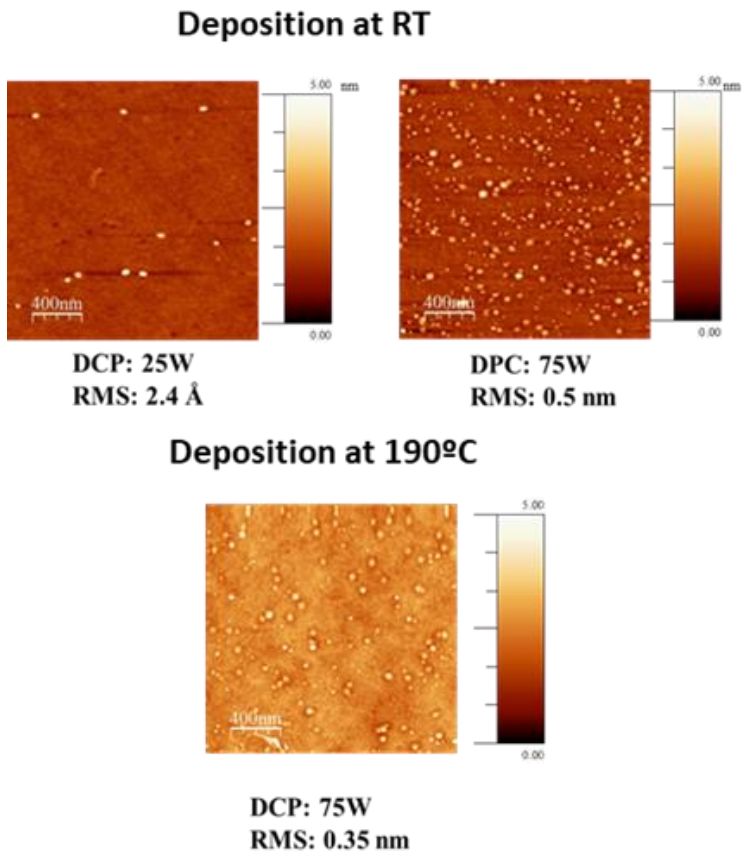


**Figure 4**. 2D surface topography images of 80nm-thick ITO film samples used as front contact in SHJ devices.

The topography images showed two different surfaces depending on the film nature: (i) a protrusion-free surface for the amorphous thin films (25W and RT), and (ii) film surfaces with many protrusions of different sizes and densities for the pc thin films (75W, RT and 190ºC).

The root-mean-square (RMS) values of the samples deposited at RT increased from 0.24 nm (amorphous sample) to 0.5 nm (pc sample). This increase in roughness with DCP was attributed to the superior kinetic energy that the sputtered particles presented at higher DCP values [26].

On the other hand, when the substrate temperature was raised to 190ºC, a slightly smoother surface was obtained than the one deposited at RT and the same DCP value of 75 W. In addition, the density of protrusions for the sample deposited at 190ºC slightly decreased compared to that deposited at RT. This was attributed to the enhanced movement of the particles due to the superior kinetic energy that the sputtered particles had at the highest substrate temperature of 190ºC used in this work [27].

**Table 3.** Sheet resistance Rsheet and average transmittance in the visible region of the 80 nm-thick ITO films, depending on the sputtering conditions and its nature.

| ITO Conditions | Film nature | $R_{sheet}$ (Ω/sqr) | T (%) |
|---|---|---|---|
| 25W, RT | Amorphous | 85 ± 5 | 87 |
| 75W, RT | Polycrystalline | 87 ± 5 | 90 |
| 75W, 190ºC | Polycrystalline | 80 ± 5 | 75 |

Table 3 shows the main optoelectronic properties of the ITO thin films used as front contact and ARC into the device. No significant difference was observed in the electrical performance, unlike the average T values. Firstly, a slight enhancement was observed in T for

the films deposited at RT when DCP was increased from 25W to 75W from 87% to 90%, attributed to the amorphous polycrystalline transition [28]. Secondly, a worsening in T was observed as a function of the substrate temperature (down to 75%), which may be a consequence of the changes in the texture observed in the XRD analysis [29].

Figure 5 pictures the total (hemispherical) reflectance (Rhem) spectra of the fabricated ITO thin films incorporated into the SHJ devices. As can be noted, the incorporation of an ITO thin film led to a considerable reduction of the Rhem values in the visible wavelength region, decreasing the value reflected on the silicon surface in all cases. This fact confirmed their role and capability as ARC to be used in the solar device. The shift of the minimum observed in the reflectance spectra was related to slight deviations in the ITO thickness from the nominal one of 80 nm.

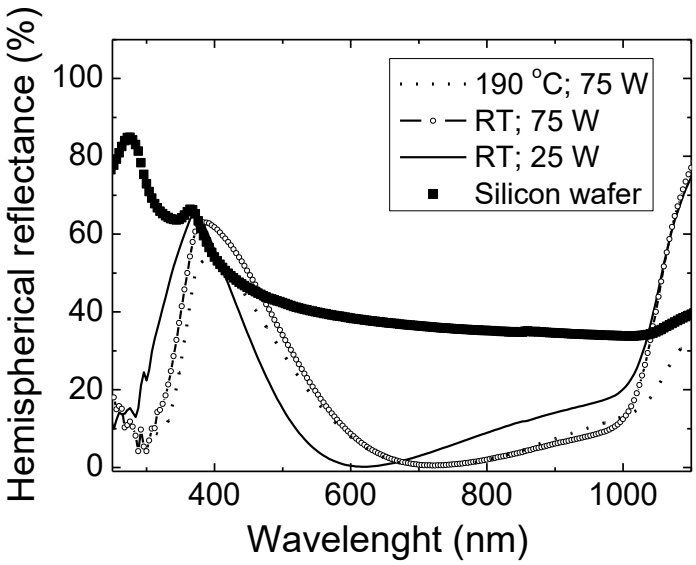


**Figure 5**. Hemispherical reflectance spectra of the ITO thin films used in the SHJ devices as front contact and ARC.

Finally, SHJ solar cells were developed by sputtering the 80 nm-thick ITO films on the front side, as previously described. Table 4 summarizes the effective minority-carrier lifetime τ and the cell implied open-circuit voltage iVoc measured with the Sinton instrument before and just after ITO sputtering process.

**Table 4.** Effective minority-carrier lifetime τ and cell implied open-circuit voltage iVoc obtained before and after ITO sputtering**.**

| | **Before** | **After** | **Before** | **After** |
|---|---|---|---|---|
| ITO Conditions | τ (μs) | τ(μs) | $iV_{oc}$ (V) | $iV_{oc}$ (V) |
| 25W, RT | 618 | 476 | 685 | 678 |
| 75W, RT | 986 | 521 | 702 | 682 |
| 75W, 190ºC | 460 | 456 | 685 | 675 |

In all cases, devices showed a reduction of the minority-carrier lifetime after ITO sputtering. RT-deposited samples showed lifetime degradation, but the effect was considerably higher for the highest DCP value. This could be explained because a low-power ITO sputtering would reduce defect formation in the a-Si layers and at the a-Si/c-Si interface, minimizing the deterioration of the effective minority-carrier lifetime upon ITO deposition, mainly near the maximum power injection levels [30]. On the other hand, the sample deposited at 190ºC showed a very low pre-sputtering lifetime. Therefore, degradation was almost negligible, making comparisons meaningless.

Table 5 summarizes the values of the Voc (finished device) and the difference with the implied-$V_{oc}$ (measured before the metal contact deposition).

**Table 5.** Difference between the implied open-circuit voltage $iV_{oc}$ obtained before and after ITO sputtering $\Delta iV_{oc}$, Voc obtained in the finished cells, and the difference between $V_{oc}$ and the implied-$V_{oc}$ measured before metal contact deposition.

| ITO Conditions | ΔiVoc (V) | Voc (V) | Voc- iVoc(V) |
|---|---|---|---|
| 25W, RT | 7 | 651 | -27 |
| 75W, RT | 20 | 667 | -15 |
| 75W, 190ºC | 10 | 643 | -32 |

As a result, the difference in iVoc before and after ITO deposition was only 7V when DCP was set at the lowest value of 25W, whereas it increased to 20V when DCP was 75W. On the other hand, the difference between iVoc performed directly on ITO without the metal contacts and the open-circuit voltage Voc, obtained after the cell finished, showed that the highest detriment was observed in the sample with an ITO layer deposited at 190ºC and 75W. In this case, substrate temperature might lead to long-term degradation of passivation layer quality after cell processing. No advantage was achieved by depositing the ITO front contact at a high substrate temperature. Therefore, the results showed less detrimental device performance when using low substrate temperatures, implying significant energy savings. This study demonstrated the relevant impact of the sputtering deposition conditions of the front contact material on the main photovoltaic parameters.

## 4. Conclusions

In this work, the double role of ITO as an effective n-doped layer in a silicon-based heterojunction and a transparent electrode/ARC in silicon PV devices was demonstrated. In all cases, the ITO thin films were sputtered using low energy consumption conditions without post-treatment. The results showed an important influence of the sputtering conditions used in its fabrication on device performance: As an n-doped layer in the heterojunction, the limiting parameter was film nature, achieving better results with amorphous thin films. On the other hand, when used as front contact and ARC in SHJ devices for our range in deposition parameters, it seems that high substrate temperature would not positively affect device performance more than power does. In any case, it has been demonstrated that ITO thin films fabricated at low energy consumption conditions can be successfully used in both roles, leading to important energy savings.

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## Conflicts of Interest

The authors declare no conflict of interest.

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